# PLANAR MAGNETIC TUNNEL JUNCTION SUBSTRATE HAVING RECESSED ALIGNMENT MARKS


## ABSTRACT

A method for forming an alignment mark structure for a semiconductor device includes forming an alignment recess at a selected level of the semiconductor device substrate. A first metal layer is formed over the selected substrate level and within the alignment recess, wherein the alignment recess is formed at a depth such that the first metal layer only partially fills the alignment recess. A second metal layer is formed over the first metal layer such that the alignment recess is completely filled. The second metal layer and the first metal layer are then planarized down to the selected substrate level, thereby creating a sacrificial plug of the second layer material within the alignment recess. The sacrificial plug is removed in a manner so as not to substantially roughen the planarized surface at the selected substrate level.